EE CprE 491 – May 20 - 49
CySat Senior Design Team
Week 7 Report

October 5 – October 11
Faculty Advisors: Phillip Jones

Team Members:

Bryan Friestad — *Team Lead / EPS Lead*
Ryan Hansen — *SDR Lead*
Chase Kirchner — *Ground Station Lead / CI Testing Lead*
Kyle Muehlenthaler — *Radio / Antenna Lead*
Talon Stromgren — *GitLab Master / Payload Lead*
Xiangzhu Yan — *ADCS Lead*

Past Week Accomplishments

- OBC: Diagnosed issues with JTAG. Found bad power pin for JTAG target VCC. Matthew will communicate with Endurosat about issues. Hold off for the time being.
- ADCS:
- SDR: Met with Brian Bradford and got an overview of SDR board setup and past dev.
- EPS: Nothing
- Payload:
- Ground Station: Getting up to speed on Ground Station documentation/processes
- UHF Antenna: nothing done

Pending Issues

- OBC: Pin 1 on connector CN1 (JTAG) incorrectly supplies 1.04V instead of 3.3V. More details below with pictures.

Individual Contributions

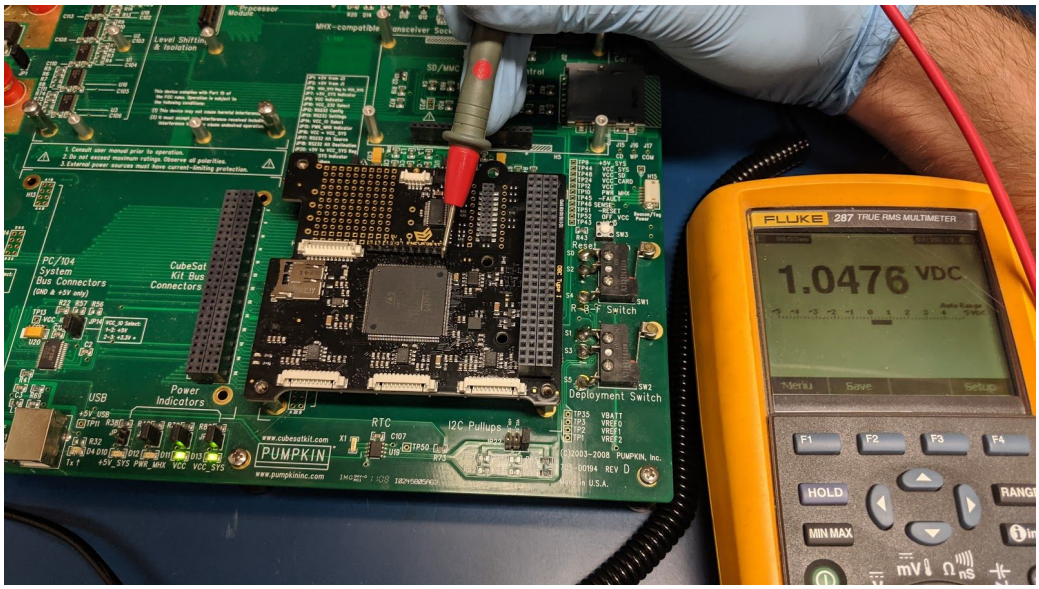
Team Member	Contribution	Weekly Hours	Total Hours
Bryan Friestad	Lightning talk, troubleshot OBC, got key for anti-static room, consolidate GIT, informed higher-ups re:OBC	3	3
Ryan Hansen	Tested OBC, Started SDR, attend gen meeting,	3	3
Chase Kirchner	Reviewing Ground Station documentation. Sent follow-up questions to Matt	2	2
Kyle Muehlenthaler	Attended meeting, Scribe,	3	3
Talon Stromgren			
Xiangzhu Yan	Attend gen meeting, read ADCS Commissioning Manual	3	3

Plans for Coming Week

- OBC:
- ADCS:
- SDR: Get started with adding UART commands to SDR code.
- EPS: Read ConOps v4 for EPS
- Payload:
- Ground Station:
- UHF Antenna:

Incorrect Target VCC

- CN1 Pin 1 incorrect voltage.
- Should be 3.3V



Temporary Voltage Test.

- Supplemented correct 3.3V from PC104 stack to Pin 1 (Target VCC) and JTAG seemed to work.
- (System powered off for picture after successful test)